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MACPHERSON KWOK CHEN & HEID LLP
2033 GATEWAY PLACE
SUITE 400
SAN JOSE, CA 95110

EXAMINER	
WASHBURN, DANIEL C	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/750,721	FERRIZ, RAFAEL MAESTRE	
	Examiner	Art Unit	
	DANIEL WASHBURN	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/2/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to because the handwritten corrections on at least Figure 2 are illegible. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Figures 1-3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct

any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The abstract of the disclosure is objected to because the inventor's name appears as the first line of the abstract, where the remainder of the abstract is a separate paragraph. The examiner respectfully requests that the inventor's name be removed from the abstract page. Correction is required. See MPEP § 608.01(b).

Claim Objections

Claims 1 and 4 are objected to because of the following informalities: Claim 1 initially describes a tap window size of N_{taps}, but later describes the variable as N_{Taps}, where the T in taps is capitalized. The examiner respectfully requests that the variable N_{taps} be consistently written throughout the claim, in order to avoid any confusion as to whether or not the same variable is being described throughout the claim.

The fourth line of claim 4 reads, "storing output words in the frame buffer for the plurality of scaled video ***lines***", it should read, "storing output words in the frame buffer for the plurality of scaled video ***lines;***", where a semicolon is included at the end of the limitation.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 10-12, 16 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Law (US 5,671,020).

RE claim 1, Law describes a method of image scaling using an array of processing elements, wherein the processing elements are arranged from a first processing element to an nth processing element (Figure 3A and 6:35-7:32 describes a prior art method and system horizontally decimating (scaling) an image using a plurality of processing elements PPE0-PPE7), and wherein the image scaling uses a tap window size of N_{taps}, (7:6-32 describes using a three tap filter) the method comprising:

(a) loading a frame buffer with pixel values from a video line, the pixel values in the loaded frame buffer being arranged into words having a width of n input pixel values (1:43-65 describes storing pixel values in raster scan format in a memory, retrieving the pixel values from the memory so the system may perform preprocessing operations, such as hierarchical decimation, and then storing the newly computed pixel values back into the memory. The described memory is considered a frame buffer as it stores, pixel by pixel, the contents of an image. Further, the pixel values are stored in raster scan format, which the examiner considers pixel values that are arranged into words having a width of some number of input pixel values); and

(b) broadcasting N_{taps} words from the loaded frame buffer to the array (1:43-65 describes that pixel data may be retrieved from the memory such that hierarchical decimation may be carried out on the pixel data),

wherein for each word, the input pixel values are arranged from a first input pixel value to an nth input pixel value such that, for each word broadcast to the array, the first processing element processes the first input pixel value in the word, the second processing element processes the second input pixel value in the word, and so on, and wherein the broadcast order of the pixel values is such that each processing element is configured to process the N_{taps} input pixels it receives from the frame buffer into a scaled output pixel value using the same multiply-and-accumulate coefficient set, the processing elements thereby producing an output word of n scaled pixel values (Figure 3A and 6:35-7:32 describes that the retrieved pixel values are stored in a memory buffer 302, where once the pixels are stored in the memory buffer 302 a crossbar network 306 directs selected pixels to the proper processing elements PPE0-PPE7. Each processing element comprises a three tap filter with coefficients k1, k2, and k3 and three consecutive pixels are provided to each of the processing elements PPE0-PPE7, one at a time, where each processing element performs a multiply and accumulate operation. Each processing element then outputs an output pixel value that is the weighted average of the input pixel values. Thus, the set of processing elements PPE0-PPE7 outputs an output word of n scaled pixel values, where in this case n=8).

RE claim 3, Law describes the method of claim 1, further comprising:

(c) repeating act (b) to produce a succession of output words from the array of processing elements, wherein the succession of output words represents a horizontally-scaled version of the video line (7:48-54 describes that the process for calculating output pixel values according to equation (1) is repeated for all pixels of each picture until all pictures are processed).

RE claim 10, Law describes an image processor, comprising:

an array of processing elements arranged from a first processing element to an nth processing element (Figure 3A and 6:35-7:32 describes PPE0-PPE3);

a frame buffer storing input words of n pixel values in length (1:43-65 describes that pixel data is stored in raster scan format in a memory such as a RAM. The pixel data can be retrieved from the RAM, preprocessed, such as a hierarchical decimation processing operation, and then stored back into the RAM. The RAM is thus considered a frame buffer, as it stores, pixel by pixel, data for an image. The RAM is also considered to store the pixel data as words having a width of some number of pixels),

the image processor being configured such that input words from the frame buffer may be successively broadcast to the array of processing elements, wherein the first processing element receives the first pixel value from a broadcast input word, the second processing element receives the second pixel value from the broadcast input word, and so on, the processing elements being configured to perform multiply-and-accumulate (MAC) operations on the received values such that after the broadcast of N_{taps} words from the frame buffer, each processing element may provide a scaled output pixel value using the same MAC coefficient set, the array of processing elements

thereby producing an output word of n scaled output pixel values (Figure 3A and 6:35-7:32 describes processing elements PPE0-PPE3, which input pixel data retrieved from memory and perform MAC operations on the received values in order to produce an output word of n scaled output pixel values).

RE claim 11, Law describes the image processor of claim 10, wherein the image processor is configured such that the output word may be stored in the frame buffer (1:43-65 describes that once the hierarchical decimation is complete the new pixel data is stored back into the memory it was retrieved from).

RE claim 12, Law describes the image processor of claim 10, wherein the output word is a horizontally-scaled output word (7:6-32 describes horizontal decimation (scaling) of the input pixel words to form an output word).

RE claim 16, Law describes the image processor of claim 10, further comprising one or more additional arrays of processing elements, the frame buffer being arranged to successively broadcast input words to the one or more additional arrays such that the one or more additional arrays may also each provide an output word of scaled pixel values, wherein each scaled pixel value in the output word from the one or more additional arrays is calculated using the same multiply-and-accumulate coefficient set (Figure 3A and 6:35-7:32 describes PPE4-PPE7, which is considered one or more additional arrays of processing elements).

RE claim 17, Law describes the image processor of claim 10, wherein the processing elements are reconfigurable processing elements (1:43-2:11 describes that the processor that contains the plurality of processing elements (PPEs) is a vector

processor or a vector computer. Further, 5:8-22 describes filter 106 (considered identical in scope to the described vector processor) as a programmable filter. Thus, the processing elements are considered to be programmable).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Law in view of Lippincott (US 6,724,948).

RE claims 2 and 14, Law describes a video filter that horizontally decimates an image (Figure 3A and 6:35-7:32), and further describes that vertical and temporal decimation are also contemplated (2:12-17).

Law doesn't describe the method of claim 1, further comprising:

vertically-scaling pixels from a set of video lines to produce scaled pixel values for the video line, wherein the pixel values loaded into the frame buffer in act (a) are the vertically-scaled pixel values, and wherein the scaled output pixel values from each processing element in act (b) are both horizontally-scaled and vertically-scaled output pixel values.

However, Lippincott describes a method comprising vertically scaling an image followed by horizontally scaling an image, wherein a four tap filter vertically scales and

stores the image and then reads the stored vertically scaled image and horizontally scales the vertically scaled image to create a final scaled image (2:45-3:35).

All the elements of claim 2 are known in Law and Lippincott, the only difference is the combination of known elements into a single system and method.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include in Law the method of vertically-scaling pixels from a set of video lines to produce scaled pixel values for the video line, wherein the pixel values loaded into the frame buffer in act (a) are the vertically-scaled pixel values, and wherein the scaled output pixel values from each processing element in act (b) are both horizontally-scaled and vertically-scaled output pixel values, as suggested by Lippincott, as this doesn't change the operation of the system disclosed in Law, and it could be used to achieve the predictable result of scaling an image both vertically and horizontally, which has the advantage that it allows the output image to be displayed on a wider range of display devices.

RE claim 13, Law describes a video filter that horizontally decimates an image (Figure 3A and 6:35-7:32), and further describes that vertical and temporal decimation are also contemplated (2:12-17).

Law doesn't describe the image processor of claim 10, wherein the output word is a vertically-scaled output word.

However, Lippincott describes a system and method of vertically scaling an image (2:45-3:35 describes vertically scaling an image, storing the scaled image, and then reading and horizontally scaling the stored vertically scaled image).

All the elements of claim 13 are known in Law and Lippincott, the only difference is the combination of known elements into a single system and method.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include in Law the system and method wherein the output word is a vertically-scaled output word, as taught by Lippincott, as this doesn't change the operation of the system disclosed in Law, and it could be used to achieve the predictable result of scaling an image both vertically and horizontally, which has the advantage that it allows the output image to be displayed on a wider range of display devices.

Claims 4, 5, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Law in view of Deierling (US 6,239,847).

RE claim 4, Law describes the method of claim 3, further comprising:

repeating acts (a) through (c) to produce a succession of output words for a plurality of horizontally-scaled video lines (7:48-54); and

storing the output words in the frame buffer for the plurality of scaled video lines (1:43-65);

Law contemplates vertically scaling images (2:12-17) but doesn't describe successively broadcasting sets of pixel values from the plurality of scaled video lines stored in the frame buffer to the array of processing elements; and

processing the sets of pixel values in the array of processing elements to produce a set of vertically-scaled output words.

However, Deierling describes horizontally scaling input pixel data, storing the scaled pixel data in memory, reading the scaled pixel data from the memory and vertically scaling the horizontally scaled pixel data to produce output data (Figure 2 and 3:37-4:6).

All the elements of claim 4 are known in Law and Deierling, the only difference is the combination of known elements into a single system and method.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include in Law successively broadcasting sets of pixel values from the plurality of (horizontally) scaled video lines stored in the frame buffer to the array of processing elements; and processing the sets of pixel values in the array of processing elements to produce a set of vertically-scaled (and horizontally scaled) output words, as taught by Deierling, as this doesn't change the operation of the system disclosed in Law, and it could be used to achieve the predictable result of scaling an image both vertically and horizontally, which has the advantage that it allows the output image to be displayed on a wider range of display devices.

RE claim 5, Law in view of Deierling doesn't describe the method of claim 4, further comprising:

re-ordering the vertically-scaled output words to provide a horizontally and vertically scaled video line.

However, if the system disclosed in Law (Figure 3A and 6:35-7:32) is used to carry out vertical scaling, where the vertically oriented input pixel words are transposed such that they are horizontally distributed among the rows in memory module 302, it

would have been obvious to one of ordinary skill in the art at the time of the invention to re-order the vertically scaled output words such that the horizontally and vertically scaled pixels are transposed back into their original vertical orientation before being stored into memory, as a horizontally and vertically scaled output image is only useful to a user if the scaled pixels are in the correct order.

RE claim 15, Law doesn't describe the image processor of claim 10, wherein the input words are horizontally-scaled words and the output words are both horizontally and vertically scaled words.

However, Deierling describes a system and method of using an n-tap filter to horizontally scale an image, and then using the same n-tap filter to input the horizontally scaled image in order to vertically scale the horizontally scaled image, which produces horizontally and vertically scaled output pixels (2:37-4:7).

See the rejection of claim 4 for rationale to combine Deierling with Law, as the same rationale applies here.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Law.

RE claim 6, Law describes the method of claim 1, wherein the number of input pixel values in the video line is an integer multiple N_i of n (7:6-32 describes that an initial 16 pixels are distributed along the bottom row of memory modules 302a-p and the next 16 pixels are distributed on a second row. Thus, the number of input pixel values in the video line of data stored in buffer 302 is 32, which is an integer multiple of the number of processing elements, which is 8 (N_i=4)), and wherein the number of output pixel values in a scaled video line is an integer multiple N_h of n (7:29-32 describes that the horizontal

decimation reduces the number of input pixels by half. Thus, the input pixels have been reduced from 32 to 16, which is an integer multiple of 8 (N_h=2)), the broadcast order in act (b) being every N_ith-1 input pixel (7:7-32 describes that three pixels are sent to each processing element in three successive broadcasts, where the third pixel of a first processing element is also the first pixel of an adjacent second processing element, thus, the broadcast order is every N_ith-1 input pixel (where N_i = 4)), the scaled output pixel values from each multiply-and-accumulate calculation cycle being spaced apart by N_h pixel values (7:19-32 describes that the three tap filter computes pixel values for every other pixel, thus the output pixels are spaced apart by N_h pixels, as the new pixels correspond to every second pixel position of the old pixels).

Law doesn't describe that the broadcast order in act (b) is every N_ith input pixel.

However, it would have been obvious to one of ordinary skill in the art at the time of the invention to include in Law a system and method wherein the broadcast order is every N_ith input pixel, as opposed to every N_ith-1 input pixel, as the applicant has not disclosed that broadcasting every N_ith pixel as opposed to broadcasting every N_ith-1 pixel to each processing element provides an advantage, solves any stated problem, or is for any particular purpose, and it appears that the device would perform equally well when broadcasting the N_ith or the N_ith-1 input pixel to each processing element, as the only difference would be the fact that broadcasting the N_ith pixel results in a 3:1 compression of the pixel data while broadcasting the N_ith-1 pixel results in a 2:1 compression of the pixel data. Accordingly, broadcasting the N_ith input pixel to each

processing element as opposed to broadcasting the N_ith-1 input pixel is deemed to be a design consideration which fails to patentably distinguish over the prior art of Law.

Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Law in view of Adams et al. (US 6,380,978).

RE claims 7 and 8, Law doesn't describe but Adams describes the method of claim 1, wherein the number of input pixel values in the video line is not an integer multiple of n or wherein the number of output pixel values in each scaled video line is not an integer multiple of n (Figures 22, 28, and 29 and 17:44-59 and 20:11-44 describes a method for filtering an image. The method includes using a processing matrix to evaluate the pixels surrounding a pixel of interest. When the processing matrix reaches a top edge or a bottom edge and no pixel data exists for some of the values required for the processing matrix the system automatically adds rows of zero data, and when the processing matrix reaches the left or right edge the system automatically copies the left-most or right-most column and extends the width of the grid of pixels, in order to compensate for the missing pixel values. The teachings in Adams can easily be applied to Law in order to compensate for situations where either the number of input pixels or the number of scaled output pixels in a video line is not an integer multiple of n.

All the elements of claims 7 and 8 are known in Law in view of Adams, the only difference is the combination of known elements into a single system and method.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to deal with the situations wherein the number of input pixel values in the

video line is not an integer multiple of n or wherein the number of output pixel values in each scaled video line is not an integer multiple of n, as described in Adams, as this doesn't change the overall operation of the system disclosed in Law, and it could be used to achieve the predictable result of a more robust scaling program that is able to automatically compensate for missing rows or columns of pixels.

RE claim 9, Law doesn't describe but Adams describes the method of claim 1, further comprising:

loading the frame buffer with padded video lines comprised of zero values, wherein when act (b) calculates output pixel values using input pixel values that are outside of the video line, zero values from the padded video lines are used (Figures 28 and 29 and 20:11-44 describes that when a top or bottom row of nonexistent pixel data is required for successful processing by the processing matrix the system automatically generates a row of zero data to act as a substitute for the nonexistent upper/lower pixel data).

See the rejection of claims 7 and 8 for rationale to combine Law with Adams, as the same rationale applies here.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Miyaguchi (US 5,600,582) describes horizontally decimating an image using an array of processing elements.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL WASHBURN whose telephone number is

(571)272-5551. The examiner can normally be reached on Monday through Friday 8:30 a.m. to 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on (571) 272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dan Washburn/
Examiner, Art Unit 2628
3/19/08

/Ulka Chauhan/
Supervisory Patent Examiner, Art Unit 2628